DOCKET NO. 98-MET-069C1 (STMI01-01012) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	David L. Isaman
Serial No.	:	09/443,160
Filed	:	November 19, 1999
For	:	SYMBOLIC STORE-LOAD BYPASS
Group No.	:	2183
Examiner	:	Idriss N. Alrobaye
Confirmation No.	:	6854

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF TRANSMISSION BY FACSIMILE

Sir:

The undersigned hereby certifies that the following documents:

1. Substitute Amendment and Response to Final Office Action

relating to the above application was faxed to (571) 270-2023 on March 22, 2010.

Date: 3/22/10 Kathy Longenecker
Faxer

Date: 3-22-2010
Daniel E. Venglarik
Reg. No. 39,409

P.O. Box 802432
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *dvenglarik@munckcarter.com*

DOCKET NO. 98-MET-069C1 (STMI01-01012) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	David L. Isaman
Serial No.	:	09/443,160
Filed	:	November 19, 1999
For	:	SYMBOLIC STORE-LOAD BYPASS
Group No.	:	2183
Examiner	:	Idriss N. Alrobaye
Confirmation No.	:	6854

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUBSTITUTE AMENDMENT AND RESPONSE TO FINAL OFFICE ACTION

Applicant withdraws the Amendment and Response to Final Office Action filed September 10, 2009 and requests amendment of the above-identified application as indicated herein. This amendment is being submitted in furtherance of prosecution of this application. Accordingly, no extension of time and no fees are believed to be required.

IN THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

.

Claim 1. (Canceled).

2. (Currently Amended) A pipelined microprocessor detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to by an instruction using identical base and offset values, wherein the first instruction is detected based upon the first base and offset address values and without computing a memory address equaling the first base address value added to the offset address ~~values~~ value in detecting the first instruction.

3. (Previously Presented) A pipelined microprocessor as claimed in claim 2 wherein the pipelined microprocessor detects a second instruction using second base and offset address values to store data into a second memory location that was previously read from, wherein the second instruction is detected based upon the second base and offset address values and without computing a memory address equaling the second base address value added to the offset address values in detecting the second instruction.

Claims 4.-5. (Canceled).

6. (Previously Presented) A pipelined microprocessor as claimed in claim 2 wherein the pipelined microprocessor examines base and offset address values used to access memory locations by store instructions that store data into the memory locations, and detects load instructions that load data from memory locations corresponding to base and offset address values identical to the base and offset address values used by the store instructions.

7. (Previously Presented) A pipelined microprocessor as claimed in claim 3 wherein the pipelined microprocessor examines base and offset address values used to access memory locations by load instructions that load data from the memory locations, and detects store instructions that store data into memory locations corresponding to base and offset address values identical to the base and offset address values used by the load instructions.

8. (Previously Presented) A pipelined microprocessor as claimed in claim 6 wherein the pipelined microprocessor detects identical offset address values and identical base address values in at least one register within the pipelined microprocessor.

9. (Previously Presented) A pipelined microprocessor as claimed in claim 7 wherein the pipelined microprocessor detects identical offset address values and identical base address values in at least one register within the pipelined microprocessor.

10. (Previously Presented) A pipelined microprocessor as claimed in claim 6 wherein the pipelined microprocessor comprises:

an instruction decode stage detecting load instructions that load data from memory locations corresponding to offset address values from an identical and base address values identical to offset address values and base address values used by prior store instructions that store data into the memory locations; and

a bypass element sending a bypass signal to an instruction execution stage of the pipelined microprocessor that indicates that a load instruction uses a base address value and an offset address value identical to a base address value and an offset address value used by a prior store instruction.

11. (Previously Presented) A pipelined microprocessor as claimed in claim 7 wherein the pipelined microprocessor comprises:

an instruction decode stage detecting store instructions that store data into memory locations using offset address values and base address values identical to offset address values and base address values used by prior load instructions that load data from memory locations; and

a bypass element sending a bypass signal to an instruction execution stage of the pipelined microprocessor that indicates that a store instruction uses a base address value and an offset address value identical to a base address value and an offset address value used by a prior load instruction.

12. (Currently Amended) A method for operating a pipelined microprocessor, comprising:

detecting, in the pipelined microprocessor, a first instruction using first base and offset address values to load data from a first memory location that was previously stored to by an instruction using identical base and offset values, wherein the first instruction is detected based upon the first base and offset address values and without computing a memory address equaling the first base address value added to the offset address ~~values~~ value in detecting the first instruction.

13. (Previously Presented) A method for operating a pipelined microprocessor as claimed in claim 12, further comprising:

detecting, in the pipelined microprocessor, a second instruction using second base and offset address values to store data into a second memory location that was previously read from, wherein the second instruction is detected based upon the second base and offset address values and without computing a memory address equaling the second base address value added to the offset address values in detecting the second instruction.

Claims 14.-15. (Canceled).

16. (Previously Presented) A method for operating a pipelined microprocessor as claimed in claim 12, further comprising:

examining, in the pipelined microprocessor, base and offset address values used to access memory locations by store instructions that store data into the memory locations; and

detecting load instructions that load data from memory locations corresponding to base and offset address values identical to the base and offset address values used by the store instructions.

17. (Previously Presented) A method for operating a pipelined microprocessor as claimed in claim 13, further comprising:

examining, in the pipelined microprocessor, base and offset address values used to access memory locations by load instructions that load data from memory locations; and

detecting said instructions that store data into memory locations corresponding to base and offset address values identical to the base and offset address values used by the load instructions.

18. (Previously Presented) A method for operating a pipelined microprocessor as claimed in claim 16, further comprising:

detecting, in an instruction decode stage of the pipelined microprocessor, load instructions that load data from memory locations corresponding to offset address values and base address values identical to offset address values and base address values used by prior store instructions that store data into the memory locations; and

sending a bypass signal from a bypass element to an instruction execution stage of the pipelined microprocessor, wherein the bypass signal indicates that a load instruction uses a base address value and an offset address value identical to a base address value and an offset address value used by a prior store instruction.

19. (Previously Presented) A method for operating a pipelined microprocessor as claimed in claim 17, further comprising:

detecting, in an instruction decode stage of the pipelined microprocessor, store instructions that store data into memory locations using offset address values and base address values identical to offset address values and base address values used by prior load instructions that load data from memory locations; and

sending a bypass signal from a bypass element to an instruction execution stage of the pipelined microprocessor, wherein the bypass signal indicates that a load instruction uses a base address value and an offset address value identical to a base address value and an offset address value used by a prior store instruction.

20. (Currently Amended) A method for operating a pipelined microprocessor, comprising:

detecting a first instruction that stores data to a first memory location, the first instruction comprising syntax for computing an effective address for the first memory location;

detecting a second instruction that loads data from a second memory location, the second instruction comprising syntax for computing an effective address for said second memory location;

determining the syntax for the first instruction and the syntax for the second instruction;

using the syntax for the first instruction and the syntax for the second instruction to determine a relationship between the first memory location and the second memory location, without using the effective address of the first memory location or the effective address of the second memory location to determine the relationship between the first memory location [[nd]] and the second memory location; and

using the relationship to determine whether to perform one of the first instruction and the second instruction.

21. (Previously Presented) A method for operating a pipelined microprocessor as claimed in claim 20, wherein the syntax for the first instruction and the syntax for the second instruction refer to an identical memory location.

REMARKS

Claims 2, 3, 6-13 and 16-21 are pending in the application.

Claims 2, 3, 6-13 and 16-21 have been rejected.

Claims 2, 12 and 20 have been amended as set forth herein.

Claims 2, 3, 6-13 and 16-21 remain pending in this application.

Reconsideration of the claims is respectfully requested. The Applicant makes the aforementioned amendments and subsequent arguments to place this application in condition for allowance.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, LLP

Date: 3-22-2010

Daniel E. Venglarik
Registration No. 39,409

P.O. Box 802432
Dallas, Texas 75380
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *dvenglarik@munckcarter.com*